Lannan Jiang

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SUMMARY

My background is in computer architecture and ASIC design, with hands-on experience contributing to multiple ASIC projects during my academic research. I completed my thesis on custom ISA extensions and processor design, demonstrating my ability to innovate in low-level hardware optimization. I have a strong passion for accelerator designs and architectures for AI/ML.

EDUCATION

ETH Zurich: MSc in Electrical Engineering and Information Technology — Sep 2021 – May 2024
Worcester Polytechnic Institute (WPI): BSc in Electrical and Computer Engineering — Sep 2017 – May 2021

SKILLS

- **Hardware Skills:** SystemVerilog, Verilog, Calibre, QuestaSim, Synopsys DC, Innovus, Virtuoso, Tetramax, Linux, Xilinx FPGA, Microcontrollers, RISC-V/x86 Assembly, ATE Testing
- **Software Skills:** C, C#, Python (Data processing, ML/DL/CV), MATLAB (DSP/Data processing), Tcl, BASH, Linux OS, OpenMP, CUDA, LaTeX, Git

RECOGNITIONS

- Bachelor of Science - High Distinction
- IEEE HKN Honor Society Member
- WPI Merit Scholarship
- Most Improved Golf Player

WORK EXPERIENCE

VLSI Teaching Assistant ***ETH Zurich - Zurich, Switzerland*** — Feb 2024 – May 2024

- Assisted 12 lab exercises covering synthesis flow, scan chain insertion, testing, timing, P&R, and backend flow
- Supported RTL-to-GDS flow tutorials using Questasim, Synopsys DC, TetraMax, Calibre, and Innovus
- Guided 70+ students through backend design flow and physical implementation exercises in Linux systems

Application Engineering Intern ***Analog Devices - Raleigh, NC, USA*** — Apr 2021 – Aug 2021

- Developed automated test systems for RF transceiver ICs using C# .NET framework, enhancing test efficiency
- Integrated multiple test instruments (e.g., DMM, spectrum analyzer, oscilloscope, RF switch box, power supply) into the NI DAQ system, streamlining power data collection and analysis
- Improved system performance by contributing to and optimizing 7000+ lines of C# code, resulting in faster, more reliable testing procedures
- Recognized for technical excellence and delivering impactful results on time by the Wireless Platform Group

Class Tutor ***Worcester Polytechnic Institute - Worcester, MA, USA*** — Sep 2020 – Dec 2020

- Instructed 2 undergraduate lab sections in Wireless Networks and Continuous-time Signal Processing
- Supervised MATLAB-based signal processing projects and provided technical guidance
- Monitored and graded midterm/final exams for 2 courses, providing detailed feedback

Central Applications Engineering Intern ***Analog Devices - Wilmington, MA, USA*** — May 2020 – Aug 2020

- Built Linux environments for RF transceiver validation, streamlining product testing workflows
- Developed FM transceiver and QPSK modem prototypes using GNURadio, enabling rapid validation of integrated transceiver
- Conducted detailed technical updates and delivered them to the team weekly

RESEARCH & THESES

Master Thesis ***ETH Zurich - Zurich, Switzerland*** — Oct 2023 – Apr 2024

Title: A RISC-V ISA Extension for Pseudo Dual-Issue Monte Carlo on Snitch

- Designed and implemented custom RISC-V ISA extensions to enable pseudo dual-issue in Snitch core for HPC
- Developed a bare-metal Monte Carlo simulation using C and assembly language with the leapfrog method to support parallel execution
- Verified ISA extensions via RTL simulation and C-based testing, ensuring full functionality and data accuracy
- Achieved significant improvements in FPU utilization (90%) and data throughput (1.4x) through targeted

microarchitectural enhancements and low-level optimizations

- Conducted extensive performance benchmarking and enabled visualization of Monte Carlo workloads using Python, yielding insights for optimization strategies and data throughput improvement

Iguana SoC Tape-Out & Physical Design ***ETH Zurich - Zurich, Switzerland*** Feb 2023 – Jun 2023

- Contributed to the first attempted open-source tape-out for 64-bit Linux-capable RISC-V Iguana SoC, a RISC-V-based chip, as part of a 12-person team using the IHP130 open-source PDK
- Led and realized physical design, achieving DRC-clean and LVS-clean layout for Iguana using commercial EDA tools (i.e. Innovus, Synopsys DC, Calibre)
- Optimized standard cells within the PDK using Virtuoso, improving timing performance and reducing chip area
- Conducted chip-level analysis to compare open-source and closed-source designs, successfully delivering the final .gds file to the foundry, meeting strict timelines

Semester Thesis ***ETH Zurich - Zurich, Switzerland*** Feb 2022 – May 2022

Title: Investigation and Integration of Floating-Point Div/Sqrt Unit

- Investigated the iterative Radix-4 SRT algorithm from OpenC906 and compared to the hard-coded Radix-2 algorithm
- Integrated a 32-bit RISC-V floating-point division and square root unit into the PULPissimo architecture for enhanced performance (github)
- Developed and executed SystemVerilog testbenches for RTL verification, ensuring compliance with IEEE-754 standards
- Implemented the synthesis process using TSMC 65nm, achieving a 46% area reduction and doubling the maximum frequency

Bachelor Thesis ***WPI - Worcester, MA, USA*** Sep 2020 – Mar 2021

Title: An Intuitive User Interface for Teleoperated Robotic Neuro-Intervention

- Conducted a literature review on surgical haptic feedback systems and selected electronic components aligned with project requirements
- Designed and developed linear and torque-based force feedback mechanisms to enable remote brain surgery using standard guide wire techniques
- Led the programming and integration of PID controllers on an Arduino Mega 2560 to acquire and process haptic feedback data
- Calibrated the system for accurate force feedback and delivered the first working prototype in collaboration with mechanical engineering peers

Independent Research: Secret Key Generation with UWB ***WPI - Worcester, MA, USA*** Mar 2020 – Sep 2020

- Generated security key pairs using channel impulse response (CIR) measured by Decawave EVK 1000
- Conducted ranging error analysis and the effects of human body obstructed line-of-sight condition on the multipath characteristics of the ranging system
- Delivered a 40-page technical report on the experiments and obtained results

ADDITIONAL CONTRIBUTIONS

Time Slot Matching WeChat Mini Program ***Chengdu, Sichuan, China*** Jan 2025 – Present

- Initiated and drove product vision for a WeChat mini program addressing group scheduling pain points
- Successfully launched the program, reaching 800+ users and validating product-market-fit

AI Copilot for Digital Circuits Design -*Zurich, Zurich, Switzerland* Mar 2024 – Jun 2024

- Conceived and contributed to the development of the proof of concept of an AI copilot for digital circuit design
- Shortlisted by Y Combinator for the first-round interview

NASA University Student Launch Initiative (USLI) - ***Huntsville, Alabama, USA*** Sep 2018 – Apr 2019

- Integrated transceivers Adafruit RFM95W LoRa for the communication systems for the payload system of the rocket
- Collaboratively designed PCB layout using Fritzing and carried out LOS/NLOS tests for performance
- Delivered design reviews to NASA and participated in on-site rocket launch

RELEVANT COURSES

- VLSI Design, Computer Architecture, System-on-Chip Data Analytics and Machine Learning, ASP/DSP, Embedded Computing, Digital Design, Wireless Networks, Microelectronics Circuits, Probabilistic AI, Computer Vision